IN THE SPECIFICATION:

Please amend the specification as follows.

Please amend the paragraph beginning at page 3, line 18, as follows.

5   In the SoC environment of the present invention, the wired-OR technique discussed above may be attempted with a passive resistor or an active transistor. FIG. 2A illustrates a passive resistor implementation, where a pull-up resistor 215 may be located off of the SoC 210 (since high tolerance resistors are difficult to build on-chip) and connected to the wired-OR network 220 through a bond pad 225. Alternatively, the resistor could be

10   implemented as either a strong always-on transistor and/or an active clamp transistor. FIGS. 2B and 2C illustrate active transistor implementations, where transistors 260, 280 may be located on of the SoC 250, 270 itself and connected to the wired-OR network 255, 275. For active transistor implementations, the strength of the pull-up device 260, 280 must be matched to the load and configuration of the wired-OR network 255, 275 such that the signal may be pulled

15   down to V_{SS} and restored to V_{DD} in one clock period. A wired-AND solution would use complementary devices and supplies <u>similar</u> to those shown in FIGS. 2A-2C.

Please amend the paragraph beginning at page 7, line 1, as follows.

FIG. 4 illustrates the relative timing of various signals on the chip 300. In the

20   following discussion, FIGS. 3 and 4 will be discussed in an integrated manner to describe the operation and relative timing of the various components and corresponding signals on the chip 300. In the example of FIG. 4, node-2 is driving the ACK signal in the first cycle, node-1 is driving the ACK signal in the second cycle and node-3 is driving the ACK signal in the fourth cycle. Thus, since there are no nodes driving the ACK signal during the third and fifth cycles,

25   the voltage level of the control signal from the previous cycle is maintained.

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